Remarks

Claims 1-6 are pending.

The drawings are objected to. Formal drawings are submitted, herewith.

Claims 1-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,330,645 of Harriman ("Harriman") in view of Chang, et al. *Array Allocation Taking Into Account SDRAM Characteristics*, Proc. of the 2000 Asia South Pacific DAC ("Chang").

Claims 1 and 2 have been amended.

Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 1-6 under 35 U.S.C. §103(a) as being unpatentable over Harriman in view of Chang. Applicants respectfully submit that claims 1-6 are not obvious in view of the combination of Harriman and Chang. It is respectfully submitted that it would be impermissible hindsight, based on applicant's own disclosure, to combine Harriman and Chang. Harriman and Chang do not teach or suggest a combination with each other. Harriman describes a multi-stream coherent memory controller apparatus and method (Harriman, title). Chang is a paper describing array allocation that takes into account SDRAM characteristics (Chang, title). Neither reference suggests a combination with the other, let alone describes the invention as claimed.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *see MPEP §2143.01.*

Neither of the cited references s provide any motivation to make the recited combination. Instead, it appears the teachings of the present application have been used as a blueprint to gather together and assemble various components of the prior art in the manner contemplated by applicants. This is a classic example of the use of hindsight reconstruction, and cannot properly be used as grounds for rejecting the present claims.

In the present case, there has been no showing of such motivation. Instead, the Examiner attempts to deconstruct the subject matter of the claims of the present application into its constituent components, states where each such component may be found in one of the cited references, and then concludes that it would have been obvious to combine the references to arrive at the claimed invention. This bare bones analysis is not sufficient to support a determination of obviousness. The burden is on the Examiner to show *why* one be so motivated as to come up with the combination being relied upon. *see MPEP §2143.01.*

In any event, even if Harriman and Chang were combined, such a combination would lack one or more features of the rejected claims. Claim 1 recites the feature of ***setting a latch*** *in said memory controller* ***to halt data transfer between said SDRAM and said processor chip*** (claim 1) (emphasis added). The Examiner has stated in part that:

> Chang teaches that "Note that two consecutive BA [bank active] commands for different banks must be separated by at least 2 cycles. After an R [read] command is performed, data is ready 3 cycles later. After a BP [bank pre-charge] command is performed, the corresponding bank does not accept any new command for 2 cycles." Examiner interprets the required pauses between commands to correspond to the claimed limitation of "halting" the transfer of data.

(Office Action, 6/3/2004, p. 5)

The cycles described in Chang used in response to the *read* and *bank pre-charge* commands do not describe "***setting a latch*** *in said memory controller* ***to halt data transfer***

between said SDRAM and said processor chip" as in claim 1. Harriman addresses data coherency and data request arbitration with large chunks of data. (Harriman, col. 4, ll. 24-29, describing the "head-of-line" blocking problem.) In particular, Harriman's arbitrator provides round robin arbitration and read write scheduling between clients. (Harriman, col. 6, ll. 47-49) Thus, Harriman's round robin service, indicates that Harriman does not contemplate and does not describe describe ***setting a latch*** *in said memory controller* ***to halt data transfer between said SDRAM and said processor chip*** as claimed in applicants' claim 1.

Chang does not disclose this claimed feature either. Chang maps arrays to different memory banks in SDRAM. (Chang, p. 1, col. 2, par. 4) As quoted above, Change describes cycles inherent with BP and R commands. (Chang, p. 2, col. 2, par. 1) Chang sends commands for new access to the SDRAM without waiting for the completion of the current access. (Chang, p. 2, col. 2, par. 1) Thus, in Chang commands perpetuate the transfer of data into and out of the SDRAM. Chang, does not describe describe ***setting a latch*** *in said memory controller* ***to halt data transfer between said SDRAM and said processor chip*** as in claim 1.

Additionally, neither Harriman nor Chang describe a "*processor chip, said processor chip including a plurality of* ***emulator processors"*** as in claim __. Chang is absolutely silent regarding this feature. Although, Harriman describes a system-on-chip having memory controllers and requestors formed on the same chip, Harriman's requestors are not "*emulator processors"* as described by applicants in claim 1.

For these reasons, the combination of Harriman and Chang lacks the features of "***setting a latch*** *in said memory controller* ***to halt data transfer between said SDRAM and said processor chip,*** *said processor chip including a plurality of emulator processors*" as stated in claim 1. Because the combination of Harriman and Chang does not disclose these features as

taught by applicants and given that claims 3 and 5 are dependent from claim 1 and add additional limitations, it is respectfully submitted that claims 1, 3, and 5 are not unpatentable under 35 U.S.C. §103(a) over Harriman in view of Chang.

The Examiner has rejected claim 2 under 35 U.S.C. §103(a) for the reason set forth in the rejection of claim 1. Amended claim 2 discloses substantially similar limitations as claim 1, and recites "***setting a latch*** *in said memory controller* ***to halt data transfer between said SDRAM and said processor chip,*** *said processor chip including a plurality of emulator processors.*" (Emphasis added) A combination of Harriman, and Chang would lack this feature for the reasons discussed above in regard to claim 1, applicants respectfully submit that claims 2, 4, and 6 are not obvious under 35 U.S.C. §103(a) by Harriman in view of Chang.

Conclusion

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (650) 614-7400. If there are any additional charges, please charge Deposit Account No. 15-0665.

Respectfully submitted,
ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: September 1, 2004 By: Sanjeet Dutta

Sanjeet K. Dutta
Reg. No. 46,145

Four Park Plaza, Suite 1600
Irvine, California 92614-2558
(650) 614-7660

OIPE
SEP 0 7 2004
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/656,541	Confirmation No.: 9916
Applicant	:	William F. Beausoleil, et al.	
Filing Date	:	September 6, 2000	
Title	:	High Speed Software Driven Emulator Comprised Of A Plurality Of Emulation Processors With A Method To Allow High Speed Bulk Read/Write Operation Synchronous DRAM While Refreshing The Memory	
Group Art Unit	:	2123	
Examiner	:	Ayal I. Sharon	
Docket No.	:	706316-1019	
Customer No.	:	34313	

RECEIVED
SEP 1 4 2004
Technology Center 2100

Commissioner for Patents
Mail Stop Non-Fee Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Applicant hereby submits formal drawing (2 sheets with 2 figures) for the above-referenced application. If there are any questions regarding these drawings, please call the undersigned.

CERTIFICATE OF MAILING
37 CFR §1.8

I hereby certify, pursuant to 37 CFR §1.8, that I have reasonable basis to expect that that this paper or fee (along with any referred to as being attached or enclosed) would be mailed or transmitted on or before the date indicated with the United States Postal Service with sufficient postage as first class mail on the date shown below in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Dated: September 1, 2004

Rita Hernandez

Applicant	:	William Beausoleil, et al.
Appl. No.	:	09/656,541
Examiner	:	Ayal I. Sharon
Docket No.	:	706316-1019

The Commissioner is authorized to charge any fee which may be required in connection with this Submission of Formal Drawings to deposit account No. 15-0665.

Respectfully submitted,
ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: September 1, 2004 By: Sanjeet Dutta
Sanjeet K. Dutta
Reg. No. 46,145

Four Park Plaza, Suite 1600
Irvine, California 92614-2558
(650) 614-7647

OIPE
SEP 0 7 2004
PATENT & TRADEMARK OFFICE

RECEIVED
SEP 1 4 2004
Technology Center 2100

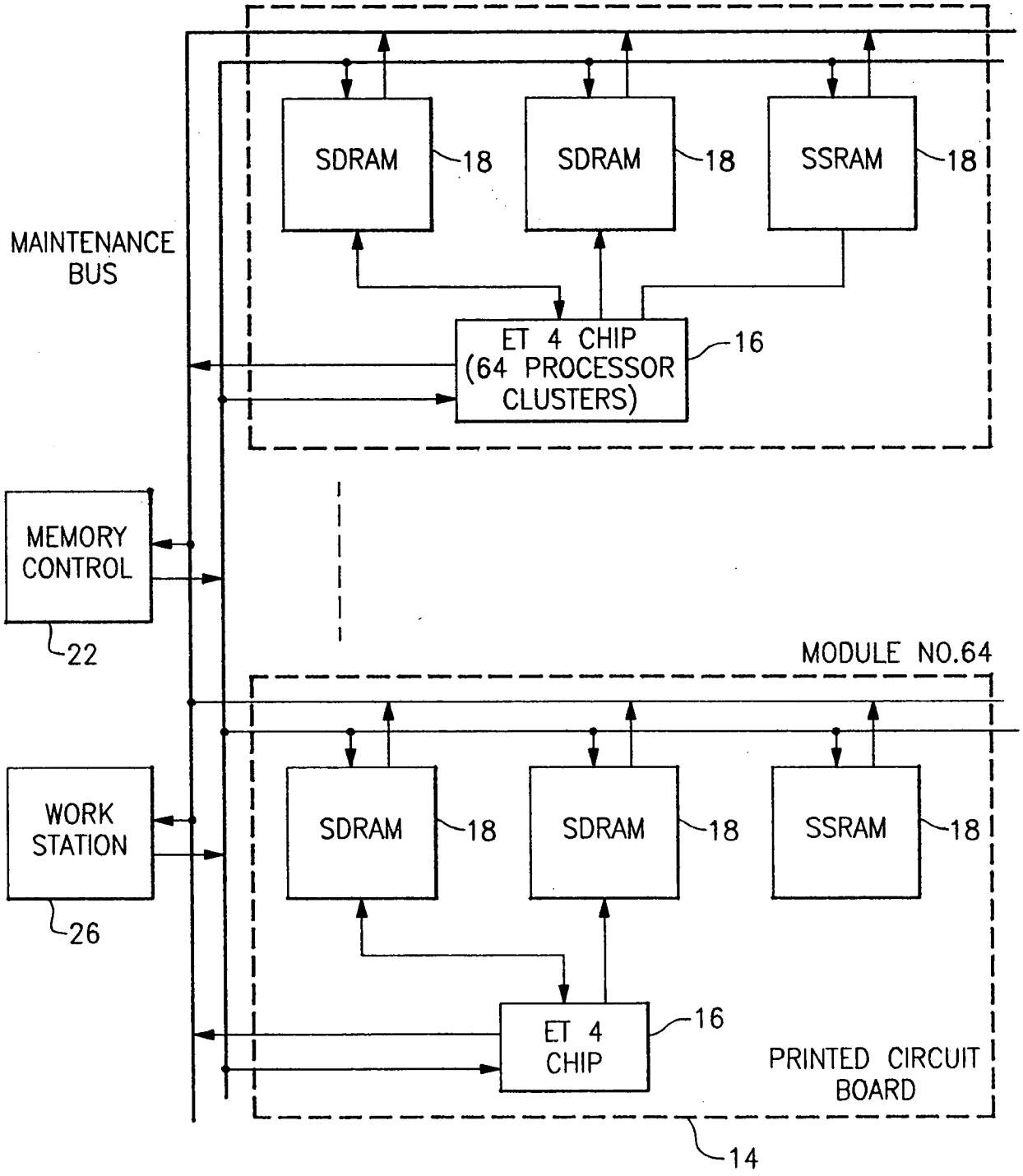

FIG.1

OIPE
SEP 0 7 2004
PATENT & TRADEMARK OFFICE

RECEIVED
SEP 1 4 2004
Technology Center 2100

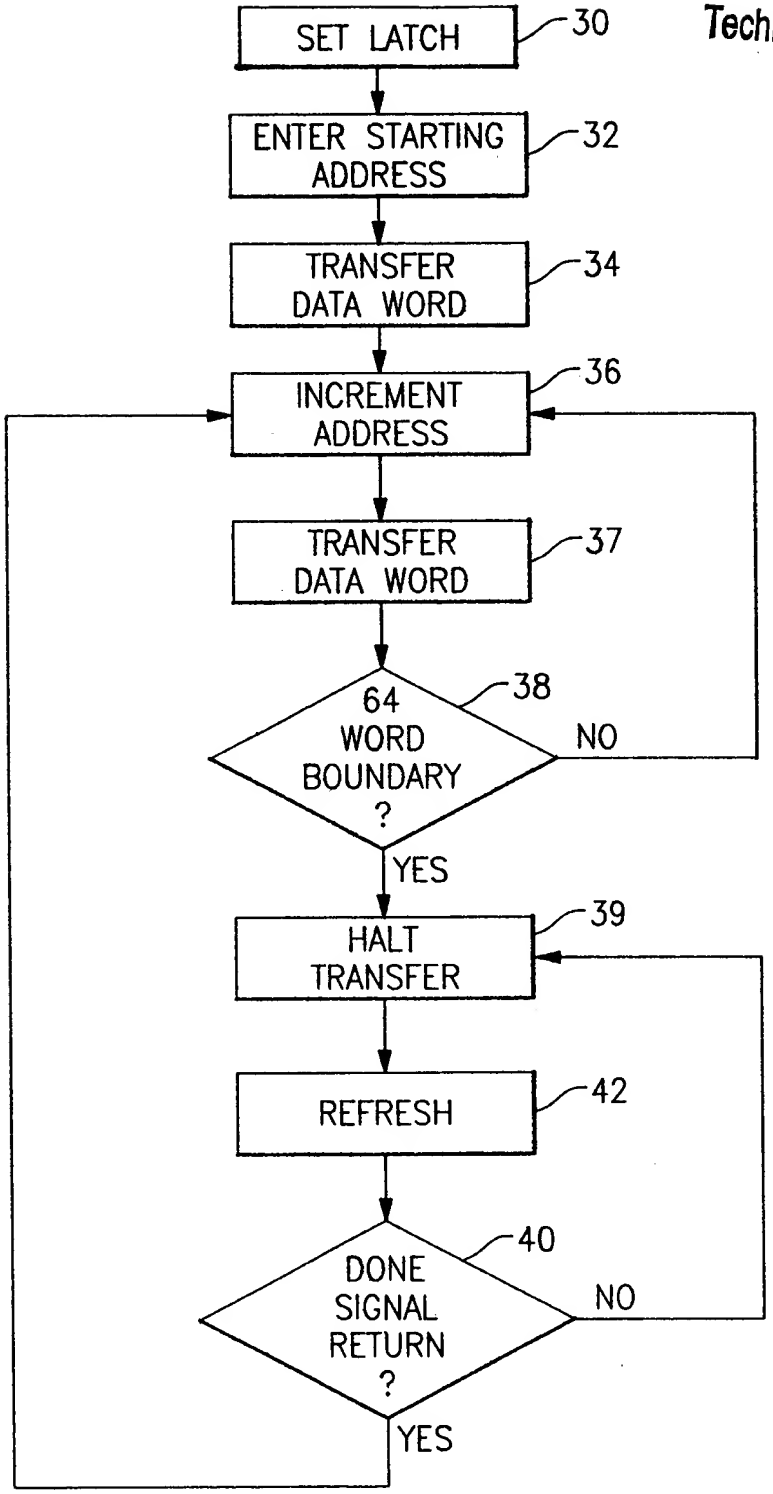

FIG.2